JXS046

2×2 56 MHz Agile RF Transceiver SoC

Product Datasheet

Revision V3.0

AD9361-Compatible RF Agile Transceiver

CONFIDENTIAL

Table of Contents

1. Applications

- Point-to-point communication systems
- Femtocell and picocell base stations (3G / 4G)
- General-purpose radio systems
- Software-defined radio (SDR) platforms
- TDD and FDD transceiver applications

2. Standards and Quality Grade

- **Detailed Specification:** JXS046 RF Agile Transceiver Detailed Specification
- **Quality Grade:** Enterprise Standard (Industrial Grade Equivalent)
- **Frequency Band:** 70 MHz to 6.0 GHz
- **Reference Device:** AD9361 (pin-compatible functional replacement)

3. Features

RF Transceiver

- RF 2×2 transceiver with integrated 12-bit DACs and ADCs
- Frequency range: 70 MHz to 6.0 GHz
- Supports both TDD and FDD operation
- Tunable channel bandwidth: less than 200 kHz to 56 MHz
- TX EVM: less than –40 dB

Power Supplies

- Core supply voltage: 1.3 V
- I/O interface supply: 1.8 V / 2.5 V
- GPO supply voltage: 3.3 V

Digital Interface

- CMOS / LVDS digital data interface
- Configurable single-port or dual-port data path
- SPI control interface (up to 30 MHz)

Reliability and Package

- ESD rating: Class 1B, HBM 500 V
- Operating temperature: –40 °C to +85 °C
- Package: 144-pin CSP_BGA, 10 mm × 10 mm
- Product weight: 0.32 g ± 0.02 g

4. Product Overview

The JXS046 is a high-performance, highly integrated RF agile transceiver designed for 3G and 4G base station applications. Its programmability and wideband capability make it an ideal choice for a broad range of transceiver applications. The device integrates an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to the baseband processor.

The JXS046 operates over a frequency range of 70 MHz to 6.0 GHz, covering most licensed and unlicensed bands. Supported channel bandwidth ranges from less than 200 kHz up to 56 MHz.

Two independent direct-conversion receivers deliver state-of-the-art noise figure and linearity. Each receive (RX) subsystem includes independent automatic gain control (AGC), DC offset correction, quadrature correction, and digital

filtering, eliminating the need to provide these functions in the digital baseband. Each channel is equipped with two high-dynamic-range ADCs that digitize the received I and Q signals and pass them through configurable decimation filters and a 128-tap FIR filter, producing 12-bit output signals at the corresponding sample rate.

The transmitter employs a direct-conversion architecture that achieves high modulation accuracy and ultra-low noise, delivering a TX EVM of less than –40 dB. The on-board transmit (TX) power monitor can be used as a power detector, enabling highly accurate TX power measurement.

Fully integrated phase-locked loops (PLLs) provide low-power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation required for FDD systems is integrated on chip. All VCO and loop filter components are also integrated.

The device is offered in a 10 mm × 10 mm, 144-pin chip-scale ball grid array (CSP_BGA) package.

(See Chinese Datasheet Page 5)

Figure 1: Functional Block Diagram

Important Notes

1. RX and TX Baseband Bandwidth Calibration

The baseband bandwidth calibration clock is derived from the master clock through a divider. The RX divider ratio is determined by Reg1F8[7:0] (BBF Tune Divide), and the TX divider ratio by Reg0D6[7:0]. This divider value must not be odd — i.e., Reg1F8[0] and Reg0D6[0] must not be set to 1. The divider value is jointly determined by the BBPLL frequency and the baseband bandwidth:

$$\text{BBF Tune Divide}[8:0] = \text{ceil}\left(\frac{\text{BBPLL Freq} \times \ln(2)}{\text{BBBW} \times 1.4 \times 2 \times \pi}\right)$$

During chip initialization, avoid setting the above two registers to 1. After initialization, verify that these register values are not 1. If the value is 1, adjust the baseband bandwidth and re-initialize the chip.

2. RX Channel I/Q Mismatch

At 1.8 GHz LO frequency and high temperature (80 °C ± 4 °C), there is a probability of I/Q mismatch in the receive channel. (Reference device exhibits mismatch at –20 °C.)

5. Package Outline and Dimensions

(See Chinese Datasheet Page 7)

Figure 2: Package Outline Drawing (Unit: mm)

Table 1. Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	1.27	1.42 *a*	1.57	e	—	0.80	—
A1	0.30	0.35 *a*	0.40	Φb	0.40	0.45 *a*	0.50
D	9.80	10.00 *a*	10.20	Z	—	0.60 *a*	0.70
E	9.80	10.00 *a*	10.20				

a — Actual nominal value of package body. Users are recommended to design with reference to this dimension.
Note: Refer to assembly guidelines for recommended pad design.

6. Pin Description

(See Chinese Datasheet Page 8)

Figure 3: Pin Arrangement (Top View)

Table 2. Pin Function Description

Pin	Symbol	Description	I/O	Pin	Symbol	Description	I/O
A1	RX2A_N	RX Ch.2 Input A Negative	I	G1	RX_EXT_LO_IN	RX Ext. LO Signal Input	I
A2	RX2A_P	RX Ch.2 Input A Positive	I	G2	RX_VCO_LDO_OUT	RX VCO LDO Output	O
A3	NC	No Connect *a*	/	G3	VDDA1P1_RX_VCO	RX VCO LDO Input	I
A4	VSSA	Analog Ground	I	G4	CTRL_OUT7	Control Output 7	O
A5	TX_MON2	TX Ch.2 Power Monitor In	I	G5	EN_AGC	AGC Manual Control In	I
A6	VSSA	Analog Ground	I	G6	ENABLE	State Machine Enable	I
A7	TX2A_N	TX Ch.2 Output A Negative	O	G7	RX_FRAME_N	RX Frame Diff. Out. Neg.	O
A8	TX2A_P	TX Ch.2 Output A Positive	O	G8	RX_FRAME_P	RX Frame Diff. Out. Pos.	O
A9	TX2B_N	TX Ch.2 Output B Negative	O	G9	TX_FRAME_P	TX Frame Diff. In Pos.	I
A10	TX2B_P	TX Ch.2 Output B Positive	O	G10	FB_CLK_N	TX Data Clock Diff. In Neg.	I
A11	VDDA1P1_TX_VCO	TX VCO Supply Input	I	G11	DATA_CLK_P	RX Data Clock Diff. Out Pos.	O
A12	TX_EXT_LO_IN	TX Ext. LO Signal Input	I	G12	VSSD	Digital Ground	I
B1	VSSA	Analog Ground	I	H1	RX1B_P	RX Ch.1 Input B Positive	I
B2	VSSA	Analog Ground	I	H2	VSSA	Analog Ground	I
B3	AUXDAC1	Auxiliary DAC 1 Output	O	H3	VSSA	Analog Ground	I
B4	GPO_3	General-Purpose Output 3	O	H4	TXNRX	ENSM TX/RX Ctrl.	I
B5	GPO_2	General-Purpose Output 2	O	H5	SYNC_IN	Sync Input	I

Pin	Symbol	Description	I/O	Pin	Symbol	Description	I/O
B6	GPO_1	General-Purpose Output 1	O	H6	VSSA	Analog Ground	I
B7	GPO_0	General-Purpose Output 0	O	H7	VSSD	Digital Ground	I
B8	VDD_GPO	Aux. DAC & GPO Supply	I	H8	P1_D11/RX_D5_P	P1 D11 / RX D5 Diff. Out+	I/O
B9	VDDA1P3_TX_LO	TX LO 1.3 V Supply	I	H9	TX_FRAME_N	TX Frame Diff. In Neg.	I
B10	VDDA1P3_TX_VCO_LDO	TX VCO LDO Supply In	I	H10	VSSD	Digital Ground	I
B11	TX_VCO_LDO_OUT	TX VCO LDO Output	O	H11	DATA_CLK_N	RX Data Clock Diff. Out Neg.	O
B12	VSSA	Analog Ground	I	H12	VDD_INTERFACE	Digital I/O Supply	I
C1	RX2C_P	RX Ch.2 Input C Positive	I	J1	RX1B_N	RX Ch.1 Input B Negative	I
C2	VSSA	Analog Ground	I	J2	VSSA	Analog Ground	I
C3	AUXDAC2	Auxiliary DAC 2 Output	O	J3	VDDA1P3_RX_SYNTH	RX Synth. 1.3 V Supply	I
C4	TEST/ENABLE	Test Input	I	J4	SPI_DI	SPI Serial Data Input	I
C5	CTRL_IN0	Control Input 0	I	J5	SPI_CLK	SPI Clock Input	I
C6	CTRL_IN1	Control Input 1	I	J6	CLK_OUT	Clock Output	O
C7	VSSA	Analog Ground	I	J7	P1_D10/RX_D5_N	P1 D10 / RX D5 Diff. Out–	I/O
C8	VSSA	Analog Ground	I	J8	P1_D9/RX_D4_P	P1 D9 / RX D4 Diff. Out+	I/O
C9	VSSA	Analog Ground	I	J9	P1_D7/RX_D3_P	P1 D7 / RX D3 Diff. Out+	I/O
C10	VSSA	Analog Ground	I	J10	P1_D5/RX_D2_P	P1 D5 / RX D2 Diff. Out+	I/O
C11	VSSA	Analog Ground	I	J11	P1_D3/RX_D1_P	P1 D3 / RX D1 Diff. Out+	I/O
C12	VSSA	Analog Ground	I	J12	P1_D1/RX_D0_P	P1 D1 / RX D0 Diff. Out+	I/O
D1	RX2C_N	RX Ch.2 Input C Negative	I	K1	RX1C_P	RX Ch.1 Input C Positive	I
D2	VDDA1P3_RX_RF	Receiver 1.3 V Supply	I	K2	VSSA	Analog Ground	I
D3	VDDA1P3_RX_TX	RX/TX 1.3 V Supply	I	K3	VDDA1P3_TX_SYNTH	TX Synth. 1.3 V Supply	I
D4	CTRL_OUT0	Control Output 0	O	K4	VDDA1P3_BB	Baseband 1.3 V Supply	I
D5	CTRL_IN3	Control Input 3	I	K5	RESETB	Reset Input (Active Low)	I
D6	CTRL_IN2	Control Input 2	I	K6	SPI_ENB	SPI Enable Input	I
D7	P0_D9/TX_D4_P	P0 D9 / TX D4 Diff. In+	I/O	K7	P1_D8/RX_D4_N	P1 D8 / RX D4 Diff. Out–	I/O
D8	P0_D7/TX_D3_P	P0 D7 / TX D3 Diff. In+	I/O	K8	P1_D6/RX_D3_N	P1 D6 / RX D3 Diff. Out–	I/O
D9	P0_D5/TX_D2_P	P0 D5 / TX D2 Diff. In+	I/O	K9	P1_D4/RX_D2_N	P1 D4 / RX D2 Diff. Out–	I/O
D10	P0_D3/TX_D1_P	P0 D3 / TX D1 Diff. In+	I/O	K10	P1_D2/RX_D1_N	P1 D2 / RX D1 Diff. Out–	I/O
D11	P0_D1/TX_D0_P	P0 D1 / TX D0 Diff. In+	I/O	K11	P1_D0/RX_D0_N	P1 D0 / RX D0 Diff. Out–	I/O
D12	VSSD	Digital Ground	I	K12	VSSD	Digital Ground	I
E1	RX2B_P	RX Ch.2 Input B Positive	I	L1	RX1C_N	RX Ch.1 Input C Negative	I

Pin	Symbol	Description	I/O	Pin	Symbol	Description	I/O
E2	VDDA1P3_RX_LO	RX LO 1.3 V Supply	I	L2	VSSA	Analog Ground	I
E3	VDDA1P3_TX_LO_BUF	TX LO Buf. 1.3 V Supply	I	L3	VSSA	Analog Ground	I
E4	CTRL_OUT1	Control Output 1	O	L4	RBIAS	Bias Reference Input	I
E5	CTRL_OUT2	Control Output 2	O	L5	AUXADC	Auxiliary ADC Input	I
E6	CTRL_OUT3	Control Output 3	O	L6	SPI_DO	SPI Serial Data Output	O
E7	P0_D11/TX_D5_P	P0 D11 / TX D5 Diff. In+	I/O	L7	VSSA	Analog Ground	I
E8	P0_D8/TX_D4_N	P0 D8 / TX D4 Diff. In–	I/O	L8	VSSA	Analog Ground	I
E9	P0_D6/TX_D3_N	P0 D6 / TX D3 Diff. In–	I/O	L9	VSSA	Analog Ground	I
E10	P0_D4/TX_D2_N	P0 D4 / TX D2 Diff. In–	I/O	L10	VSSA	Analog Ground	I
E11	P0_D2/TX_D1_N	P0 D2 / TX D1 Diff. In–	I/O	L11	VSSA	Analog Ground	I
E12	P0_D0/TX_D0_N	P0 D0 / TX D0 Diff. In–	I/O	L12	VSSA	Analog Ground	I
F1	RX2B_N	RX Ch.2 Input B Negative	I	M1	RX1A_P	RX Ch.1 Input A Positive	I
F2	VDDA1P3_RX_VCO_LDO	RX VCO LDO Supply In	I	M2	RX1A_N	RX Ch.1 Input A Negative	I
F3	VSSA	Analog Ground	I	M3	NC	No Connect *a*	/
F4	CTRL_OUT6	Control Output 6	O	M4	VSSA	Analog Ground	I
F5	CTRL_OUT5	Control Output 5	O	M5	TX_MON1	TX Ch.1 Power Monitor In	I
F6	CTRL_OUT4	Control Output 4	O	M6	VSSA	Analog Ground	I
F7	VSSD	Digital Ground	I	M7	TX1A_P	TX Ch.1 Output A Positive	O
F8	P0_D10/TX_D5_N	P0 D10 / TX D5 Diff. In–	I/O	M8	TX1A_N	TX Ch.1 Output A Negative	O
F9	VSSD	Digital Ground	I	M9	TX1B_P	TX Ch.1 Output B Positive	O
F10	FB_CLK_P	TX Data Clock In Pos.	I	M10	TX1B_N	TX Ch.1 Output B Negative	O
F11	VSSD	Digital Ground	I	M11	XTALP	Ref. Crystal / Ext. Clock In	I
F12	VDDD1P3_DIG	1.3 V Digital Supply	I	M12	XTALN	Ref. Crystal Connection	I

a — No connect. Leave this pin unconnected in application.

7. Recommended Operating Conditions

All specifications at T_A = 25 °C, nominal supply voltages, unless otherwise noted.

Parameter	Min	Typ	Max	Unit
Input Reference Clock	—	40	—	MHz
Analog/Digital Core Supply (VDDX)	—	1.3	—	V
Interface Supply (VDD_INTERFACE)	1.71	1.8 / 2.5	2.625	V
GPO Supply (VDD_GPO)	—	3.3	—	V
Operating Ambient Temperature (T_A)	–40	—	+85	°C

8. Absolute Maximum Ratings

Stresses exceeding absolute maximum ratings may cause permanent damage. These are stress ratings only; functional operation at these conditions is not implied.

Parameter	Min	Max	Unit
Analog/Digital Core Supply to Ground (VDDx to VSSx)	–0.3	1.4	V
Interface Supply to Ground (VDD_INTERFACE to VSSx)	–0.3	3.0	V
GPO Supply to Ground (VDD_GPO to VSSx)	–0.3	3.9	V
Logic I/O to Ground (VSSx)	–0.3	VDD_INTERFACE + 0.3	V
Input Current on Any Pin (except supply pins)	±10	±10	mA
RF Input (Peak Power)	—	2.5	dBm
TX Monitor Input Power (Peak)	—	9	dBm
Package Power Dissipation	—	$(T_{JMAX} - T_A) / \theta_{JA}$	W
Maximum Junction Temperature (T_{JMAX})	—	110	°C
Storage Temperature (T_{stg})	–65	+150	°C

9. Electrical Characteristics

Unless otherwise specified: $V_{DDA1P3\_RX\_LO}$ = 1.3 V, $V_{DDA1P3\_TX\_LO}$ = 1.3 V, $V_{DDA1P3\_RX\_RF}$ = 1.3 V, $V_{DDA1P3\_RX\_TX}$ = 1.3 V, $V_{DDA1P3\_TX\_LO\_BUFFER}$ = 1.3 V, $V_{DDA1P3\_RX\_SYNTH}$ = 1.3 V, $V_{DDA1P3\_TX\_SYNTH}$ = 1.3 V, V_{DDA1P3_BB} = 1.3 V, V_{DDD1P3_DIG} = 1.3 V, V_{DD_GPO} = 3.3 V, $V_{DD\_INTERFACE}$ = 1.8 V, V_{SSD} = V_{SS} = 0 V, internal LO mode, –40 °C ≤ T_A ≤ 85 °C.

9.1 Receiver — Frequency-Independent Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Center Frequency	F_0	RX1A / RX2A	70	—	6000	MHz
Gain Control Range	Gain_Range	800 MHz	—	71.5	—	dB
		2300 MHz (RX1A, RX2A)	—	70	—	dB
		2300 MHz (RX1B, RX2B, RX1C, RX2C)	—	70	—	dB
		5500 MHz (RX1A, RX2A)	—	62	—	dB
Gain Step	GS	—	—	1	—	dB
RSSI Range	RSSI_Range	RX1A / RX2A	—	95	—	dB
RSSI Accuracy	—	—	—	±2.5	—	dB

9.2 Receiver — 800 MHz Band

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise Figure	NF	Max. RX Gain	—	2.0	—	dB
Input Third-Order Intercept	IIP3	RX1A/RX2A, Max. RX Gain	—	–11	—	dBm
Input Second-Order Intercept	IIP2	RX1A/RX2A, Max. RX Gain	—	55	—	dBm
Digital Domain LO Leakage	LOL	At RX Front End	—	–82	—	dBm
Quadrature Gain Error	—	—	—	0.2	—	%
Quadrature Phase Error	—	—	—	0.2	—	deg
Modulation Accuracy (EVM)	EVM_RX	—	—	N/T *a*	—	—
Input Return Loss (S11)	—	—	—	N/T *a*	—	dB
RX1A to RX2A Isolation	ISO_RX	—	—	68	—	dB
RX1C to RX2C Isolation	ISO_RX	—	—	68	—	dB
RX1B to RX2B Isolation	ISO_RX	—	—	55	—	dB
RX2A to RX1A Isolation	ISO_RX	—	—	68	—	dB
RX2C to RX1C Isolation	ISO_RX	—	—	68	—	dB
RX2B to RX1B Isolation	ISO_RX	—	—	55	—	dB

9.3 Receiver — 2.4 GHz Band

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise Figure	NF	Max. RX Gain	—	3.5	—	dB
Input Third-Order Intercept	IIP3	RX1A/RX2A, Max. RX Gain	—	–10	—	dBm
Input Second-Order Intercept	IIP2	RX1A/RX2A, Max. RX Gain	—	48	—	dBm
Digital Domain LO Leakage	LOL	At RX Front End	—	–82	—	dBm
Quadrature Gain Error	—	—	—	0.2	—	%
Quadrature Phase Error	—	—	—	0.2	—	deg
RX1A to RX2A Isolation	ISO_RX	—	—	55	—	dB
RX1C to RX2C Isolation	ISO_RX	—	—	55	—	dB
RX1B to RX2B Isolation	ISO_RX	—	—	50	—	dB
RX2A to RX1A Isolation	ISO_RX	—	—	55	—	dB
RX2C to RX1C Isolation	ISO_RX	—	—	55	—	dB
RX2B to RX1B Isolation	ISO_RX	—	—	50	—	dB

9.4 Receiver — 5.5 GHz Band

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise Figure	NF	Max. RX Gain	—	4.0	—	dB
Input Third-Order Intercept	IIP3	RX1A/RX2A, Max. RX Gain	—	–4	—	dBm
Input Second-Order Intercept	IIP2	RX1A/RX2A, Max. RX Gain	—	58	—	dBm
Digital Domain LO Leakage	LOL	At RX Front End	—	–75	—	dBm
Quadrature Gain Error	—	—	—	0.2	—	%
Quadrature Phase Error	—	—	—	0.2	—	deg
RX1A to RX2A Isolation	ISO_RX	—	—	50	—	dB
RX2A to RX1A Isolation	ISO_RX	—	—	37	—	dB

9.5 Transmitter — Frequency-Independent Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Center Frequency	F_0	TX1A / TX2A	70	—	6000	MHz
Power Control Range	PCR	TX1A / TX2A	—	90	—	dB
Power Control Resolution	PRes	TX1A / TX2A	—	0.25	—	dB

9.6 Transmitter — 800 MHz Band

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Return Loss (S22)	—	—	—	N/T *a*	—	dB
Max Output Power	P_O	1 MHz Tone, 50 Ω Load	—	8	—	dBm
Modulation Accuracy (EVM)	EVM_TX	19.2 MHz Ref. Clock	—	–45	—	dB
Output Third-Order Intercept	OIP3	—	—	17	—	dBm
Carrier Leakage	CL	0 dB Attenuation	—	–50	—	dBc
		40 dB Attenuation	—	–40	—	dBc
Noise Spectral Density	NSD	TX1A/TX2A, @ 90 MHz Offset	—	–148	—	dBm/Hz
TX1 to TX2 Isolation	ISO_TX	—	—	50	—	dB
TX2 to TX1 Isolation	ISO_TX	—	—	50	—	dB

9.7 Transmitter — 2.4 GHz Band

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Max Output Power	P_O	1 MHz Tone, 50 Ω Load	—	7	—	dBm
Modulation Accuracy (EVM)	EVM_TX	40 MHz Ref. Clock	—	–40	—	dB
Output Third-Order Intercept	OIP3	—	—	17.5	—	dBm
Carrier Leakage	CL	0 dB Attenuation	—	–50	—	dBc
		40 dB Attenuation	—	–44	—	dBc
Noise Spectral Density	NSD	TX1A/TX2A, @ 90 MHz Offset	—	–138	—	dBm/Hz
TX1 to TX2 Isolation	ISO_TX	—	—	50	—	dB
TX2 to TX1 Isolation	ISO_TX	—	—	50	—	dB

9.8 Transmitter — 5.5 GHz Band

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Max Output Power	P_O	7.7 MHz Tone, 50 Ω Load	—	4.2	—	dBm
Modulation Accuracy (EVM)	EVM_TX	40 MHz Ref. Clock	—	–34.5	—	dB
Output Third-Order Intercept	OIP3	—	—	13	—	dBm
Carrier Leakage	CL	0 dB Attenuation	—	–50	—	dBc
		40 dB Attenuation	—	–42	—	dBc
Noise Spectral Density	NSD	TX1A/TX2A, @ 90 MHz Offset	—	–137	—	dBm/Hz
TX1 to TX2 Isolation	ISO_TX	—	—	50	—	dB
TX2 to TX1 Isolation	ISO_TX	—	—	50	—	dB

a — Not tested. Typical values are measured at room temperature.

10. Typical Performance Characteristics

T_A = 25 °C, nominal supply voltages, typical values shown.

(See Chinese Datasheet Page 8)
Figure 4: LO Phase Noise — 800 MHz Band

(See Chinese Datasheet Page 14)
Figure 5: LO Phase Noise — 2.4 GHz Band

(See Chinese Datasheet Page 14)
Figure 6: LO Phase Noise — 5.5 GHz Band

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Figure 7: TX EVM — 800 MHz Band

(See Chinese Datasheet Page 15)
Figure 8: TX EVM — 2.4 GHz Band

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Figure 9: TX EVM — 5.5 GHz Band

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Figure 10: TX Max Output Power — 800 MHz

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Figure 11: TX Max Output Power — 2.4 GHz

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Figure 12: TX Max Output Power — 5.5 GHz

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Figure 13: RX Noise Figure vs. Frequency

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Figure 14: RX Gain vs. Control Code

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Figure 15: TX Output Power vs. Attenuation

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Figure 16: Current Consumption vs. Bandwidth

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Figure 17: Typical Application Schematic

11. Functional Description

11.1 Principle of Operation

The JXS046 is a high-performance, highly integrated RF agile transceiver designed for 3G and 4G base station applications. The device integrates all necessary RF, mixed-signal, and digital modules, providing complete transceiver functionality in a single chip. Its programmability enables this wideband transceiver to adapt to multiple communication standards, supporting both FDD and TDD operation.

The device also provides self-calibration and AGC systems to maintain high performance across varying temperature and input signal conditions. Multiple test modes are included, allowing system designers to inject test tones and create internal loopback paths during prototyping to debug designs and optimize radio configurations.

11.2 Receiver

The receiver features a direct-conversion architecture with differential analog inputs. Each receive (RX) subsystem includes independent automatic gain control (AGC), DC offset correction, quadrature correction, and digital filtering, eliminating the need for these functions in the digital baseband. Each channel is equipped with two high-dynamic-range 12-bit ADCs that digitize the received I and Q signals and pass them through configurable decimation filters and a 128-tap FIR filter, producing 12-bit output signals at the corresponding sample rate.

11.3 Transmitter

The transmitter employs a direct-conversion architecture that achieves high modulation accuracy and ultra-low noise, delivering TX EVM of less than –40 dB. The on-board transmit (TX) power monitor can be used as a power detector, enabling highly accurate TX power measurement. The TX path includes upconversion, filtering, and power amplifier driver stages. The transmitter supports both FDD and TDD modes of operation.

11.4 Clock Input Options

The reference clock can be provided by either a crystal oscillator connected across the XTALP/XTALN pins, or an external oscillator/clock source connected to XTALP. The internal synthesizers generate all required data clocks and sampling clocks.

The default reference clock frequency is 40 MHz. The device supports a wide range of reference clock frequencies, with the synthesizer automatically configuring the appropriate dividers and multipliers.

11.5 Frequency Synthesizer

The device includes fully integrated fractional-N frequency synthesizers for both receiver and transmitter paths, providing fast frequency hopping capability. Fully integrated PLLs deliver low-power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation required for FDD systems is integrated on chip. All VCO and loop filter components are also integrated.

11.6 Digital Data Interface

The device supports both CMOS and LVDS digital data interfaces, with configurable single-port or dual-port operation. The SPI interface provides access to all control and configuration registers. The data interface supports DDR and SDR modes, with configurable data clock frequencies up to 245.76 MHz in LVDS mode.

11.7 DATA_CLK Signal

The DATA_CLK signal is the output data clock for the receive path and the input reference clock (FB_CLK) for the transmit path. In CMOS mode, DATA_CLK operates at up to 61.44 MHz. In LVDS mode, DATA_CLK operates at up to 245.76 MHz, supporting higher bandwidth configurations such as the 56 MHz bandwidth mode (P-P56).

12. Register Information

The JXS046 includes a comprehensive register set accessible via the SPI interface. All device functions — including frequency synthesis, gain control, filter configuration, calibration, and digital interface settings — are controlled through internal registers.

- RX and TX frequency control registers
- RX and TX gain control registers
- Baseband filter tuning registers (e.g., Reg1F8 for RX BBF, Reg0D6 for TX BBF)
- Digital interface configuration registers
- Synthesizer and VCO calibration registers
- AGC control registers
- GPO and control I/O registers
- Auxiliary ADC and DAC control registers

For detailed register descriptions and address maps, refer to the JXS046 Register Map document. The SPI interface supports both 3-wire and 4-wire modes, with a maximum clock frequency of 30 MHz.

13. Power Supply and ESD Protection

13.1 Power Supply Decoupling

Proper power supply decoupling is critical for optimal device performance. Each supply pin should have a local decoupling capacitor placed as close to the pin as possible.

- Each 1.3 V supply pin: 0.1 µF ceramic capacitor to ground
- Each interface supply pin (1.8 V / 2.5 V): 0.1 µF ceramic capacitor
- 3.3 V GPO supply: 0.1 µF + 1 µF ceramic capacitors
- LDO output pins: use low-ESR decoupling capacitors as recommended
- A large PCB ground plane is recommended for optimal thermal and noise performance

13.2 ESD Protection

All pins incorporate ESD protection structures. The ESD rating is Class 1B (HBM 500 V). High-energy electrostatic pulses may still damage the device. Proper ESD handling precautions must be observed during all stages of handling and assembly.

14. Assembly and Handling Notes

14.1 Product Installation Notes

- Verify device orientation before soldering — pin 1 indicator must align with PCB mark
- Use standard BGA reflow profiles appropriate for the package size
- Ensure all supply pins are properly connected; do not leave any VDD or VSS pin floating
- Do not reverse supply polarity or short I/O pins to supply rails
- All test instruments must share a common ground connection

14.2 Product Usage Notes

- Do not operate the device beyond the absolute maximum ratings
- Proper thermal management must be ensured at maximum power dissipation conditions
- Follow recommended initialization and calibration sequences during power-up
- The RESETB pin must be held low during power supply ramp-up
- RX and TX baseband bandwidth calibration dividers must not be set to odd values

14.3 Product Handling and Protection Notes

- Observe proper ESD handling procedures at all times
- Moisture Sensitivity Level: MSL 3
- After removal from moisture barrier bag: max. 168 h floor life at ≤30 °C / 60% RH before reflow
- If storage conditions cannot be controlled, bake at 125 °C for 8 hours before assembly
- After baking, complete soldering within 12 hours if ambient exceeds 30 °C / 60% RH
- After baking, the product is particularly prone to static charge buildup

14.4 Assembly Instructions

Pay attention to device orientation during soldering to avoid misalignment. Standard BGA reflow profiles are recommended. Refer to the recommended pad design in the assembly guidelines. The recommended solder mask defined pad diameter is 0.40 mm for a 0.45 mm nominal ball diameter.

15. Troubleshooting

Symptom	Possible Cause	Suggested Remedy
Device does not respond to SPI	Incorrect SPI connection or timing	Verify SPI_CLK, SPI_ENB, SPI_DI connections; check SPI timing
No RX output data	Improper initialization or clock issues	Verify reference clock; check register initialization sequence
High RX noise figure	AGC not configured; input matching issue	Verify AGC settings; check RX input matching network
Low TX output power	Gain setting too low; calibration error	Check TX attenuation registers; run TX calibration
I/Q mismatch observed	High temperature with certain LO frequencies	Enable I/Q correction; avoid known problem frequency/temp regions
Excessive current consumption	Unused blocks not powered down	Verify power-down registers for unused channels/blocks
BBF calibration fails	Divider ratio is odd (Reg1F8[0] or Reg0D6[0] = 1)	Adjust bandwidth setting slightly and re-initialize
Clock output not present	CLK_OUT register not enabled	Enable CLK_OUT via SPI register

16. Comparison with Reference Device (AD9361)

16.1 Summary Comparison

Parameter	JXS046	AD9361 (Reference)	Comparison
Package	BGA144	BGA144	Consistent
Quality Grade	Enterprise Standard	Industrial Grade	Equivalent
Frequency Range	70 MHz – 6.0 GHz	70 MHz – 6.0 GHz	Consistent
Channel Bandwidth	Up to 56 MHz	Up to 56 MHz	Consistent
Package Size	10 mm × 10 mm	10 mm × 10 mm	Consistent
Supply Voltages	1.3 / 1.8 / 3.3 V	1.3 / 1.8 / 3.3 V	Consistent
Digital Interface	CMOS / LVDS	CMOS / LVDS	Consistent
Replacement Type	Functional Replacement	—	Pin-compatible

16.2 DC Characteristics Comparison

Parameter	Conditions	AD9361 Min	AD9361 Typ	AD9361 Max	JXS046 Min	JXS046 Max	Unit	Comparison
CMOS Logic 1 Input V	CMOS mode, P0/P1	0.65×VDD	—	—	0.7×VDD	—	V	Conservative
CMOS Logic 0 Input V	CMOS mode, P0/P1	—	—	0.35×VDD	—	0.3×VDD	V	Conservative
CMOS Input Leakage	CMOS mode, P0/P1	–10	—	10	–10	10	µA	Consistent
CMOS Logic 1 Output V	CMOS mode, P0/P1	0.8×VDD	—	—	0.8×VDD	—	V	Consistent
CMOS Logic 0 Output V	CMOS mode, P0/P1	—	—	0.2×VDD	—	0.2×VDD	V	Consistent
LVDS Input Voltage Range	—	825	—	1575	825	1575	mV	Consistent
LVDS Input Diff. Threshold	—	–100	—	100	–100	100	mV	Consistent
LVDS Input Diff. Resistance	—	—	100	—	80	120	Ω	JXS046 specifies limits
LVDS Output High Level	—	—	—	1375	1300	—	mV	Register-dependent
LVDS Output Low Level	—	1025	—	—	—	1150	mV	Register-dependent
LVDS Output Amplitude	—	150	—	—	150	—	mV	Consistent
LVDS Output Common Mode	—	—	1200	—	1100	1300	mV	JXS046 specifies limits
GPO Output High Level	VDD_GPO = 3.3 V	0.8×VDD	—	—	0.8×VDD	—	V	Consistent
GPO Output Low Level	VDD_GPO = 3.3 V	—	—	0.2×VDD	—	0.2×VDD	V	Consistent
SPI Clock Max. Frequency	—	—	—	—	—	30	MHz	New parameter
GPO Output Current	—	—	10	—	8	12	mA	JXS046 specifies limits

16.3 SPI Timing Comparison

Parameter	Conditions	AD9361 Min	AD9361 Typ	AD9361 Max	JXS046 Min	JXS046 Max	Unit	Comparison
SPI_CLK Period	—	20	—	—	33	—	ns	JXS046 max. is lower
SPI_CLK Pulse Width	—	9	—	—	16	—	ns	Half of 33 ns period
SPI_ENB Setup to SPI_CLK↑	—	1	—	—	1	—	ns	Consistent
SPI_CLK↓ to SPI_ENB Hold	—	0	—	—	0	—	ns	Consistent
SPI_DI Setup to SPI_CLK	—	2	—	—	2	—	ns	Consistent
SPI_DI Hold to SPI_CLK	—	1	—	—	1	—	ns	Consistent
SPI_CLK↑ to Data Output Delay	4-wire mode	3	—	8	3	15	ns	Wider range
	3-wire mode	3	—	8	3	15	ns	Wider range
Bus Turnaround (Read)	After address bit	tH	—	tCO max	—	—	ns	Design-guaranteed
Bus Turnaround (Read)	After data bit	—	—	tCO max	—	—	ns	Design-guaranteed

16.4 Digital Data Timing (CMOS, 1.8 V)

Parameter	Conditions	AD9361 Min	AD9361 Typ	AD9361 Max	JXS046 Min	JXS046 Max	Unit	Comparison
DATA_CLK Period	61.44 MHz	16.276	—	—	16.276	—	ns	Consistent
DATA_CLK Pulse Width	—	tCP×0.45	—	tCP×0.55	tCP×0.45	tCP×0.55	ns	Consistent
FB_CLK Pulse Width	—	tCP×0.45	—	tCP×0.55	—	—	ns	Measured higher
TX Data Setup to FB_CLK	TX_FRAME, P0/P1	1	—	—	—	—	ns	Not in spec
TX Data Hold to FB_CLK	—	0	—	—	—	—	ns	Not in spec
DATA_CLK to Data Out Delay	—	0	—	1.5	0	1.5	ns	Consistent
DATA_CLK to RX_FRAME Delay	—	0	—	1.0	0	1.5	ns	Slightly higher
Pulse Width Enable	—	tCP	—	—	—	—	ns	Function-verified
Pulse Width TXNRX	FDD Indep. ENSM	tCP	—	—	—	—	ns	Function-verified
TXNRX Setup to ENABLE	TDD ENSM	0	—	—	—	—	ns	—
Bus Turnaround Before RX	TDD	2×tCP	—	—	—	—	ns	—
Bus Turnaround After RX	TDD	2×tCP	—	—	—	—	ns	—
Capacitive Load	—	—	3	—	—	—	pF	—
Capacitive Input	—	—	3	—	—	—	pF	—

16.5 Digital Data Timing (LVDS)

Parameter	Conditions	AD9361 Min	AD9361 Typ	AD9361 Max	JXS046 Min	JXS046 Max	Unit	Comparison
DATA_CLK Period	245.76 MHz	4.069	—	—	4.069	—	ns	Consistent
DATA_CLK & FB_CLK PW	—	tCP×0.45	—	tCP×0.55	tCP×0.4	tCP×0.55	ns	JXS046 min. lower
TX Data Setup to FB_CLK	TX_FRAME, TX_D	1	—	—	—	—	ns	Not in spec
TX Data Hold to FB_CLK	—	0	—	—	—	—	ns	Not in spec
DATA_CLK to Data Out Delay	—	0.25	—	1.25	0.15	1.0	ns	JXS046 delay lower
DATA_CLK to RX_FRAME Delay	—	0.25	—	1.25	0.15	1.0	ns	JXS046 delay lower
Pulse Width Enable	—	tCP	—	—	—	—	ns	Function-verified
Pulse Width TXNRX	FDD Indep. ENSM	tCP	—	—	—	—	ns	Function-verified

16.6 Supply Characteristics Comparison

Parameter	Conditions	AD9361 Min	AD9361 Typ	AD9361 Max	JXS046 Min	JXS046 Max	Unit	Comparison
1.3 V Supply Voltage	—	1.267	1.3	1.33	1.24	1.36	V	JXS046 wider range
VDD_INTERFACE (CMOS)	—	1.14	—	2.625	—	—	V	Same range
VDD_INTERFACE (LVDS)	—	1.71	—	2.625	—	—	V	Same range
VDD_INTERFACE Tolerance	All settings	–5	—	5	—	—	%	Same
VDD_GPO Range	Unused: 1.3 V min	1.3	—	3.3	—	—	V	Same
VDD_GPO Tolerance	All settings	–5	—	5	—	—	%	Same
Sleep Mode Power	—	—	0.55	—	—	20	mW	Relaxed for temp/voltage

16.7 Current Consumption — TDD Mode Summary

Configuration	Conditions	AD9361 Typ.	Unit	Notes
1R Enabled, 800 MHz	5 MHz BW, continuous RX	180	mA	FDD = highest power
1R Enabled, 800 MHz	10 MHz BW, continuous RX	210	mA	
1R Enabled, 800 MHz	20 MHz BW, continuous RX	260	mA	
2R Enabled, 800 MHz	5 MHz BW, continuous RX	265	mA	
2R Enabled, 800 MHz	10 MHz BW, continuous RX	315	mA	
2R Enabled, 800 MHz	20 MHz BW, continuous RX	405	mA	
1T Enabled, 800 MHz	5 MHz BW, 7 dBm TX	340	mA	
1T Enabled, 800 MHz	20 MHz BW, 7 dBm TX	400	mA	
2T Enabled, 800 MHz	5 MHz BW, 7 dBm TX	550	mA	FDD = highest power
2T Enabled, 800 MHz	20 MHz BW, 7 dBm TX	660	mA	
1R Enabled, 2400 MHz	5 MHz BW, continuous RX	175	mA	
2R Enabled, 2400 MHz	20 MHz BW, continuous RX	390	mA	
1T Enabled, 2400 MHz	20 MHz BW, 7 dBm TX	410	mA	
2T Enabled, 2400 MHz	20 MHz BW, 7 dBm TX	690	mA	
1R Enabled, 5500 MHz	5 MHz BW, continuous RX	175	mA	
2R Enabled, 5500 MHz	40 MHz BW, continuous RX	445	mA	
1T Enabled, 5500 MHz	40 MHz BW, 7 dBm TX	490	mA	
2T Enabled, 5500 MHz	40 MHz BW, 7 dBm TX	820	mA	Highest power mode

16.8 Current Consumption — FDD Mode Summary

Configuration	Conditions	AD9361 Typ.	Unit	Notes
1R1T Enabled, 800 MHz	5 MHz BW, 7 dBm TX	490	mA	2R2T = highest
1R1T Enabled, 800 MHz	20 MHz BW, 7 dBm TX	615	mA	
2R2T Enabled, 800 MHz	5 MHz BW, 7 dBm TX	790	mA	
2R2T Enabled, 800 MHz	20 MHz BW, 7 dBm TX	1020	mA	
1R1T Enabled, 2400 MHz	10 MHz BW, 7 dBm TX	540	mA	
2R2T Enabled, 2400 MHz	5 MHz BW, 7 dBm TX	820	mA	
2R2T Enabled, 2400 MHz	20 MHz BW, 7 dBm TX	1050	mA	JXS046 max: 1.5 W
1R1T Enabled, 5500 MHz	5 MHz BW, 7 dBm TX	550	mA	
2R2T Enabled, 5500 MHz	5 MHz BW, 7 dBm TX	895	mA	Highest condition
2R2T Enabled, 5500 MHz	20 MHz BW	—	W	JXS046 max: 1.5 W

16.9 Interface Current Summary

Mode	Configuration	1.2 V Typ.	1.8 V Typ.	2.5 V Typ.	Unit
Sleep	—	45 µA	84 µA	150 µA	µA
1R1T DDR	LTE10 SE 30.72 MHz CMOS	2.9	4.5	6.5	mA
1R1T DDR	LTE20 Diff. 30.72 MHz CMOS	5.2	8.0	11.5	mA
2R2T DDR	LTE3 Diff. 7.68 MHz CMOS	1.3	2.0	3.0	mA
2R2T DDR	LTE10 SE 61.44 MHz CMOS	4.6	8.0	11.5	mA
2R2T DDR	LTE20 Diff. 61.44 MHz CMOS	8.2	14.0	20.0	mA
2R2T DDR	P-P56 75 mV 240 MHz LVDS	14.0	14.0	26.0	mA
2R2T DDR	P-P56 300 mV 240 MHz LVDS	35.0	35.0	45.0	mA
2R2T DDR	P-P56 450 mV 240 MHz LVDS	47.0	47.0	58.0	mA

Note: AD9361 values are typical from the reference datasheet. JXS046 specifications include appropriate margins for three-temperature operation. FDD mode has the highest power consumption and is used as the worst-case test condition.

17. Additional Information

17.1 Product Status

■ Production — This product model is currently in production; standard production lead times apply.

17.2 Revision History

Revision	Date	Description
V1.20260714	2026-07-14	Initial release
V3.0	Current	Revised English datasheet with full specifications and comparison tables

17.3 Ordering Information

For ordering information, availability, and pricing, please contact your local sales representative or authorized distributor.

17.4 Disclaimer

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