JXA011

Dual-Channel, 14-Bit, 1000 MSPS A/D Converter

Product Datasheet / User Manual

Applications

- Mobile communication receivers
- Antenna array positioning, radar systems
- General-purpose software-defined radio
- Ultra-wideband satellite receivers
- Instrumentation and measurement

Standards and Quality Grade

Quality grade: Industrial grade

Semiconductor Integrated Circuit — JXA011 Series Dual-Channel 14-Bit 1000 MSPS A/D Converter Detailed Specification.

1. Features

- Sample rate: 1000 MSPS
- Supports multi-chip synchronization
- Supports IF signal sampling up to 2 GHz
- Integrated digital wideband decimation filter and NCO, supporting multi-band receivers
- SERDES serial output interface up to 10 Gbps
- Product weight: 0.22 g ± 0.02 g
- Moisture sensitivity level: MSL3

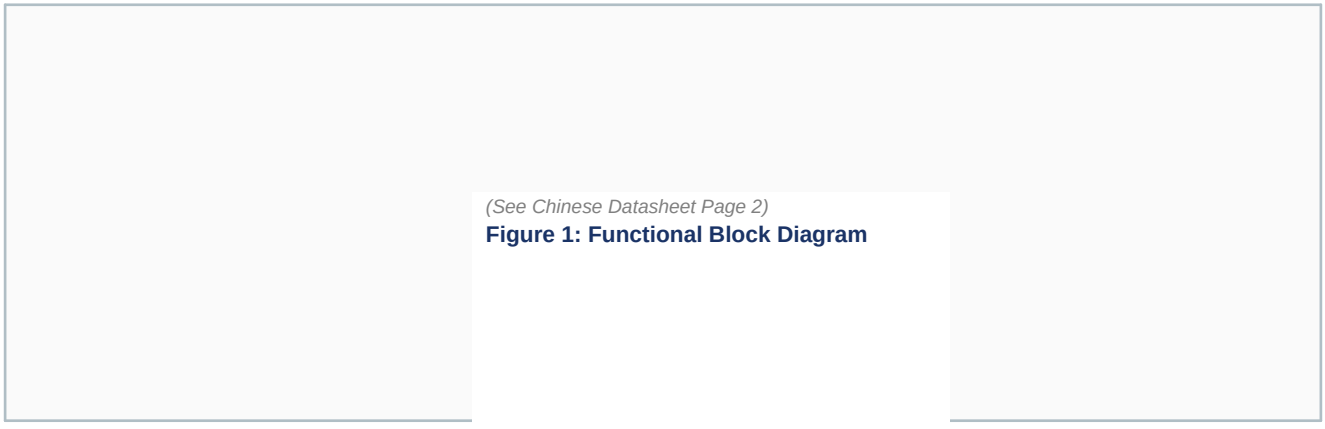
2. Product Overview

The JXA011 is a 14-bit, 1000 MSPS analog-to-digital converter (ADC) in a QFN64 package. Its functional block diagram is shown in Figure 1. The device features integrated on-chip buffer and sample-and-hold circuits, designed for low power consumption, small form factor, and ease of use. The JXA011 is optimized for wide input bandwidth, high sampling rates, excellent linearity, and low power consumption in a compact package.

The dual-channel ADC core employs a multi-stage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide-bandwidth inputs supporting various user-selectable input ranges. An integrated voltage reference simplifies system design. Both the analog input and clock signals are differential. Each ADC data output is internally connected to two digital down-converters (DDCs). Each DDC contains four cascaded signal processing stages: a 12-bit numerically controlled oscillator (NCO) and four half-band decimation filters.

In addition to the DDC modules, the device includes features that simplify automatic gain control (AGC) in communication receivers. Using the fast-detect output bit of the ADC, a programmable threshold detector can monitor input signal power. If the input signal level exceeds the programmable threshold, the fast-detect indicator goes high. Because the delay of this threshold indicator is extremely short, the user can quickly reduce system gain to avoid overdriving the ADC input.

Users can configure the JESD204B Subclass 1 high-speed serial output for 1, 2, or 4 lanes, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multi-device synchronization support is provided through the SYSREF± and SYNCINB± input pins.



(See Chinese Datasheet Page 2)

Figure 1: Functional Block Diagram

3. Package Outline and Dimensions

The device is available in a 64-lead plastic quad flat no-lead (QFN64) package. The package outline dimensions are specified in Figure 2 and Table 1.

(See Chinese Datasheet Page 3)

Figure 2: Package Outline Drawing (Unit: mm)

Table 1: Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	0.60	0.80	1.00	L	0.30	0.40	0.50
A3	—	0.20	—	D	8.90	9.00	9.10
b	0.20	0.25	0.30	E	8.90	9.00	9.10
e	—	0.50	—	D1	7.50	7.60	7.70
Z	—	0.90	—	E1	7.50	7.60	7.70

Unit: mm

4. Pin Description

The pin arrangement is shown in bottom view. The JXA011 is in a QFN64 package and is pin-compatible with the ADI AD9680.

(See Chinese Datasheet Page 4)

Figure 3: Pin Arrangement (Bottom View)

Table 2: Pin Function Description

Pin No.	Symbol	Name / Description	Pin No.	Symbol	Name / Description
—	EPAD	Exposed pad. Must be connected to ground for proper operation.	33	DGND	Digital ground
1	VAVDD1	Analog supply 1	34	VDVDD	Digital supply

Pin No.	Symbol	Name / Description	Pin No.	Symbol	Name / Description
2	VAVDD1	Analog supply 1	35	SDIO	SPI data serial input/output
3	VAVDD2	Analog supply 2	36	SCLK	SPI serial clock
4	VAVDD3	Analog supply 3	37	CSB	SPI chip select (active low)
5	VIN(A)–	Channel A analog input, negative	38	VSPIVDD	SPI digital supply
6	VIN(A)+	Channel A analog input, positive	39	VAVDD2	Analog supply 2
7	VAVDD3	Analog supply 3	40	VAVDD2	Analog supply 2
8	VAVDD2	Analog supply 2	41	VAVDD2	Analog supply 2
9	VAVDD2	Analog supply 2	42	VAVDD3	Analog supply 3
10	VAVDD2	Analog supply 2	43	VIN(B)+	Channel B analog input, positive
11	VAVDD2	Analog supply 2	44	VIN(B)–	Channel B analog input, negative
12	V1P0	1.0 V reference input / No connect. Can be configured via SPI as NC or input. Leave NC when using internal reference. 1.0 V reference input required when using external reference.	45	VAVDD3	Analog supply 3
13	VSPIVDD	SPI digital supply	46	VAVDD2	Analog supply 2
14	PDWN/STBY	Power-down input (active high). Operation depends on SPI mode; configurable as power-down or standby. External 10 kΩ pull-down resistor required.	47	VAVDD1	Analog supply 1
15	VDVDD	Digital supply	48	VAVDD1	Analog supply 1
16	DGND	Digital ground	49	VAVDD1	Analog supply 1
17	FD_A	Channel A fast-detect output	50	VAVDD2	Analog supply 2
18	DRGND	Digital driver ground	51	VAVDD2	Analog supply 2
19	VDRVDD	Digital driver supply	52	VAVDD1	Analog supply 1
20	SYNCINB–	JESD204B LVDS active-low sync input, negative	53	CLK+	ADC main clock input, positive
21	SYNCINB+	JESD204B LVDS active-low sync input, positive	54	CLK–	ADC main clock input, negative
22	SERDOUT0–	Lane 0 data output, negative	55	VAVDD1	Analog supply 1
23	SERDOUT0+	Lane 0 data output, positive	56	AGND	SYSREF+ ground reference
24	SERDOUT1–	Lane 1 data output, negative	57	VAVDD1_SR	Sync circuit analog supply
25	SERDOUT1+	Lane 1 data output, positive	58	SYSREF+	Sync reference clock, positive
26	SERDOUT2–	Lane 2 data output, negative	59	SYSREF–	Sync reference clock, negative
27	SERDOUT2+	Lane 2 data output, positive	60	AGND	SYSREF+ ground reference
28	SERDOUT3–	Lane 3 data output, negative	61	VAVDD1	Analog supply 1
29	SERDOUT3+	Lane 3 data output, positive	62	VAVDD2	Analog supply 2
30	VDRVDD	Digital driver supply	63	VAVDD2	Analog supply 2
31	DRGND	Digital driver ground	64	VAVDD1	Analog supply 1
32	FD_B	Channel B fast-detect output			

5. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency (clock)	fCLK	—	—	1000	MHz
Analog supply voltage (VAVDD1)	VAVDD1	1.22	1.25	1.28	V
Analog supply voltage (VAVDD2)	VAVDD2	2.44	2.50	2.56	V
Analog supply voltage (VAVDD3)	VAVDD3	3.2	3.3	3.4	V
SYSREF supply voltage (VAVDD1_SR)	VAVDD1_SR	1.22	1.25	1.28	V
Digital supply voltage (VDVDD)	VDVDD	1.22	1.25	1.28	V
Driver supply voltage (VDRVDD)	VDRVDD	1.22	1.25	1.28	V
SPI supply voltage (VSPIVDD)	VSPIVDD	1.7	1.8	2.0	V
Input signal amplitude (peak-to-peak)	VIN(P-P)	—	—	1.7	V
Operating temperature (case)	TC	–55	—	105	°C

6. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional operation at these or any other conditions beyond those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating	Unit
VAVDD1 to VAGND voltage	1.32	V
VAVDD1_SR to VAGND voltage	1.32	V
VAVDD2 to VAGND voltage	2.75	V
VAVDD3 to VAGND voltage	3.63	V
VDVDD to VDGND voltage	1.32	V
VDRVDD to VDRGND voltage	1.32	V
VSPIVDD to VAGND voltage	3.63	V
VAGND to VDRGND voltage	–0.3 to +0.3	V
VIN(A)+ to VAGND voltage	3.2	V
VIN(B)+ to VAGND voltage	3.2	V
SCLK, SDIO, CSB to VAGND voltage	–0.3 to VSPIVDD+0.3	V
PDWN/STBY to VAGND voltage	–0.3 to VSPIVDD+0.3	V
Thermal resistance (θJC)	4.7	°C/W
Junction temperature (TJ)	125	°C
Storage temperature (TSTG)	–55 to +125	°C
Lead solder temperature (10 s)	300	°C

7. Electrical Characteristics

Unless otherwise noted: VAVDD1 = 1.25 V, VAVDD2 = 2.5 V, VAVDD3 = 3.3 V, VAVDD1_SR = 1.25 V, VDVDD = 1.25 V, VDRVDD = 1.25 V, VSPIVDD = 1.8 V, AGND = DGND = DRGND = 0 V, –40°C ≤ TC ≤ 85°C.

Table 3: Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Typ @25°C	Unit
Resolution	RES	—	14	—	14	Bits
Sample rate	FS	—	—	1000	1000	MSPS
Number of channels	NCH	—	2	—	2	CH
Power consumption	PW	—	—	4.0	3.3	W
Differential nonlinearity	DNL	—	–2.0	+2.0	±0.8	LSB
Integral nonlinearity	INL	—	–12	+12	±2.5	LSB
Reference output voltage	VREF	—	950	1050	1000	mV
Signal-to-noise ratio	SNR	fIN = 10 MHz	60.0	—	66.8	dBFS
		fIN = 170 MHz	59.5	—	66.5	dBFS
		fIN = 450 MHz	59.2	—	64.0	dBFS
		fIN = 765 MHz	59.1	—	62.8	dBFS
Signal-to-noise and distortion	SNDR	fIN = 10 MHz	59.5	—	66.6	dBFS
		fIN = 170 MHz	59.0	—	65.8	dBFS
		fIN = 450 MHz	58.0	—	62.7	dBFS
		fIN = 765 MHz	57.5	—	62.1	dBFS
Effective number of bits	ENOB	fIN = 10 MHz	9.59	—	10.77	Bits
		fIN = 170 MHz	9.50	—	10.63	Bits
		fIN = 450 MHz	9.34	—	10.12	Bits
		fIN = 765 MHz	9.25	—	9.97	Bits
Spurious-free dynamic range	SFDR	fIN = 10 MHz	70	—	88.0	dBFS
		fIN = 170 MHz	69	—	82.0	dBFS
		fIN = 450 MHz	66	—	79.0	dBFS
		fIN = 765 MHz	66	—	77.0	dBFS
Second/third harmonic	HD2,3	fIN = 10 MHz	—	–70	–88.0	dBFS
		fIN = 170 MHz	—	–69	–82.0	dBFS
		fIN = 450 MHz	—	–66	–79.0	dBFS
		fIN = 765 MHz	—	–66	–77.0	dBFS
JESD204B interface rate	fSERDES	—	—	10	10	Gbps
Logic input high voltage	VIH	—	0.8 × VSPIVDD	—	—	V
Logic input low voltage	VIL	—	0	0.5	—	V
Logic output high voltage	VOH	—	0.8 × VSPIVDD	—	—	V
Logic output low voltage	VOL	—	0	0.5	—	V
Analog supply 1 current	IAVDD1	—	—	—	670	mA
Analog supply 2 current	IAVDD2	—	—	—	670	mA
Analog supply 3 current	IAVDD3	—	—	—	140	mA
Sync circuit supply current	IAVDD1_SR	—	—	—	10	mA
Digital supply current	IDVDD	—	—	—	200	mA
Digital driver supply current	IDRVDD	—	—	—	195	mA

Characteristic	Symbol	Condition	Min	Max	Typ @25°C	Unit
SPI digital supply current	ISPIVDD	—	—	—	5	mA

8. Typical Performance Characteristics

The following figures show typical performance characteristics of the JXA011 under nominal operating conditions.

(See Chinese Datasheet Page 4)

Figure 4: FFT Spectrum (fIN = 10 MHz)

(See Chinese Datasheet Page 5)

Figure 5: FFT Spectrum (fIN = 170 MHz)

(See Chinese Datasheet Page 6)

Figure 6: FFT Spectrum (fIN = 450 MHz)

(See Chinese Datasheet Page 8)

Figure 7: FFT Spectrum (fIN = 765 MHz)

(See Chinese Datasheet Page 11)

Figure 8: DNL and INL Curves

9. Functional Description

9.1 Typical Application Circuit

(See Chinese Datasheet Page 11)

Figure 9: Typical Application Circuit

9.2 ADC Architecture

The JXA011 consists of a dual-channel pipelined ADC. The input buffer is designed to provide termination impedance to the analog input signal. This termination impedance can be changed via SPI to match the termination requirements of the driver/amplifier. The default termination value is set to 400 Ω. The equivalent circuit of the analog input termination is shown in Figure 10. The input buffer is optimized for high linearity, low noise, and low power consumption. The input buffer provides a linear high input impedance and reduces ADC kickback.

The quantized outputs of each stage are combined to form the final 14-bit conversion result in the digital correction logic. The pipelined architecture allows the first stage to process a new input sample while the other stages continue processing previous samples.

(See Chinese Datasheet Page 12)

Figure 10: Analog Input Equivalent Circuit

9.3 Analog Input Considerations

The analog inputs of the JXA011 are differential buffers. The internal common-mode voltage of the buffer is 2.05 V. The input circuit switches between sample mode and hold mode based on the clock signal. When the input circuit switches to sample mode, the signal source must be able to charge the sampling capacitor and settle within half a clock cycle. A small series resistor at each input helps reduce peak transient currents injected from the driver output stage.

For best dynamic performance, the source impedance driving VIN+x must match the source impedance driving VIN–x to ensure symmetric common-mode settling errors. These errors are attenuated by the ADC's common-mode rejection. The internal reference buffer forms the differential reference, which in turn determines the ADC core range. In a differential configuration, setting the ADC to full-scale range achieves the highest SNR performance. For the JXA011, the available range is programmable from 1.46 V p-p to 1.94 V p-p differential via the SPI port; the default value is 1.70 V p-p differential.

9.4 Differential Input Configuration

There are various active or passive methods to drive the JXA011; however, driving the analog inputs differentially provides the best performance. In applications where SNR and SFDR are critical parameters, a differential transformer-coupled configuration (Figure 11) is recommended, as most amplifiers do not have sufficient noise performance to realize the true capability of the JXA011. For higher frequencies in the second or third Nyquist zone, it is best to remove some front-end passive components (see Table 4) to ensure wideband operation.

(See Chinese Datasheet Page 12)

Figure 11: Differential Transformer-Coupled Configuration

Table 4: Front-End Passive Component Configuration

Sample Rate	Input Frequency Range	Transformer	R1 (Ω)	R2 (Ω)	R3 (Ω)	C1 (pF)	C2 (pF)
1000 MSPS	DC to 500 MHz	ETC1-1-13 / BAL-0006SMG	25	25	10	4	2
	500 MHz to 2 GHz	BAL-0006 / BAL-0006SMG	25	25	0	Open	Open

9.5 Input Common-Mode Voltage

The JXA011 analog inputs are internally biased to common-mode. The common-mode buffer has a limited range; if the common-mode voltage drops by more than 100 mV, performance degrades significantly. Therefore, in dc-coupled applications, the common-mode voltage should be set to 2.05 V ± 100 mV to ensure proper ADC operation. When operating in dc-coupled mode, the full-scale voltage must be set to 1.7 V p-p differential.

9.6 Analog Input Control and SFDR Optimization

The JXA011 provides flexible analog input controls, such as input termination, buffer current, and input full-scale adjustment. Using Register 0x018, the buffer current of each channel can be adjusted to optimize SFDR for different input frequencies and target bandwidths. After setting the input buffer current, the current required by the AVDD3 supply changes. In some high-frequency applications, reducing the full-scale setting can improve SFDR. Table 5 provides recommended buffer current and full-scale voltage settings for different analog input frequency ranges.

Table 5: Buffer Current and Full-Scale Voltage Settings

Part Number	Frequency Range	0x018	0x019	0x01A	0x11A	0x935	0x025	0x030	0x016	0x934
JXA011-500	DC–250 MHz	0x20 (2.0×)	0x60	0x0A	0x00	0x04	0x0C (2.06 V)	0x04	0x0C/0x1C...	0x1F
	250–500 MHz	0x70 (4.5×)	0x60	0x0A	0x00	0x04	0x0C (2.06 V)	0x04	0x0C/0x1C...	0x1F
	500 MHz–1 GHz	0x80 (5.0×)	0x40	0x08	0x00	0x00	0x08 (1.46 V)	0x18	0x0C/0x1C...	0x1F or 0x00
	1–2 GHz	0xF0 (8.5×)	0x40	0x08	0x00	0x00	0x08 (1.46 V)	0x18	0x0C/0x1C...	0x1F or 0x00
JXA011-1000	DC–150 MHz	0x10 (1.5×)	0x50	0x09	0x00	0x04	0x0A (1.70 V)	0x18	0x0E/0x1E...	0x1F
	DC–500 MHz	0x40 (3.0×)	0x50	0x09	0x00	0x04	0x0A (1.70 V)	0x18	0x0E/0x1E...	0x1F
	500 MHz–1 GHz	0xA0 (6.0×)	0x60	0x09	0x20	0x00	0x08 (1.46 V)	0x18	0x0E/0x1E...	0x1F or 0x00
	1–2 GHz	0xD0 (7.5×)	0x70	0x09	0x20	0x00	0x08 (1.46 V)	0x18	0x0E/0x1E...	0x1F or 0x00
JXA011-1250	DC–625 MHz	0x50 (3.5×)	0x50	0x09	0x00	0x04	0x0A (1.70 V)	0x18	0x0E/0x1E...	0x1F
	625 MHz–2 GHz	0xA0 (6.0×)	0x50	0x09		0x00	0x08 (1.46 V)	0x18	0x0E/0x1E...	0x1F or 0x00

9.7 Voltage Reference

The JXA011 has a built-in, stable, and accurate 1.0 V voltage reference. This internal 1.0 V reference is used to set the full-scale input range of the ADC. The full-scale input range can be adjusted via ADC function register 0x025. Figure 12 shows the control block diagram of the internal 1.0 V voltage reference.

(See Chinese Datasheet Page 12)

Figure 12: Voltage Reference Configuration and Control

Via SPI register 0x024, the user can select either this internal 1.0 V reference or provide an external 1.0 V reference. When using an external reference, a 1.0 V reference source must be provided. Full-scale adjustment is done via SPI, independent of the reference voltage. Figure 13 shows how to provide an external 1.0 V reference to the JXA011.

(See Chinese Datasheet Page 13)

Figure 13: External Reference Configuration

9.8 Clock Input Considerations

To fully realize the performance of the device, a differential signal should be used as the clock signal at the JXA011 sampling clock inputs (CLK+ and CLK–). Typically, this signal should be ac-coupled to the CLK+ and CLK– pins using a transformer or clock driver. The CLK+ and CLK– pins are internally biased and require no additional biasing. Figure 14 shows a preferred method of providing the clock signal using an RF transformer to convert a single-ended signal from a low-jitter clock source to a differential signal.

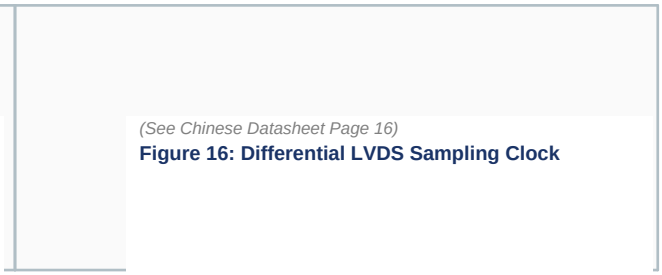
(See Chinese Datasheet Page 14)

Figure 14: Transformer-Coupled Differential Sampling Clock

Alternatively, differential CML or LVDS signals can be ac-coupled to the sampling clock input pins, as shown in Figure 15 and Figure 16.

(See Chinese Datasheet Page 14)

Figure 15: Differential CML Sampling Clock



(See Chinese Datasheet Page 16)

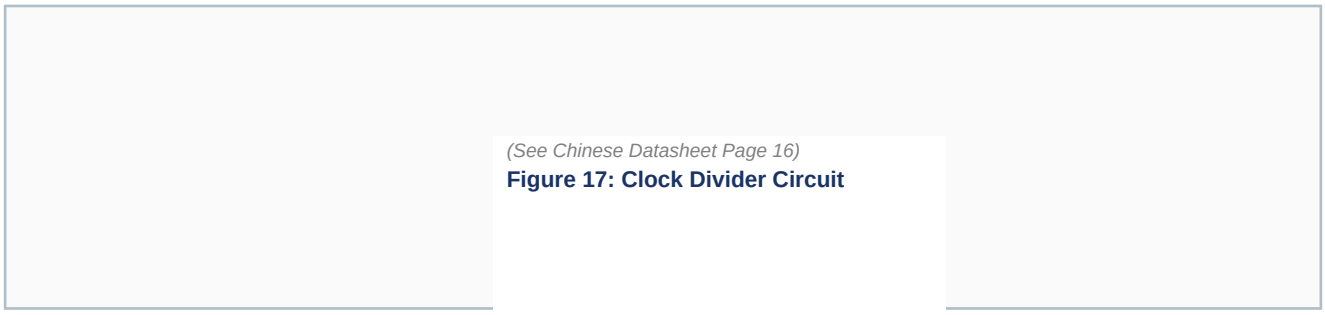
Figure 16: Differential LVDS Sampling Clock

9.9 Clock Duty Cycle Considerations

Typical high-speed ADCs use both clock edges to generate different internal timing signals and can therefore be sensitive to clock duty cycle. Generally, to maintain the dynamic performance of the ADC, the clock duty cycle tolerance should be 5%. In applications where a 50% clock duty cycle cannot be guaranteed, a higher multiple-frequency clock can be provided to the device. When the internal clock divider is set to 2, the JXA011 can accept a 2 GHz clock. The divider output provides a 50% duty cycle, high-slew-rate clock signal to the internal ADC.

9.10 Input Clock Divider

The JXA011 includes an input clock divider that can divide the Nyquist input clock by 1, 2, 4, or 8. The division ratio can be selected via register 0x10B. The maximum frequency of the CLK± inputs is 4 GHz, which is the limit of the divider. In applications where the clock input is a multiple of the sampling clock, the clock divider ratio must be set carefully before applying the clock signal to ensure controlled current transients during device startup.



(See Chinese Datasheet Page 16)

Figure 17: Clock Divider Circuit

The JXA011 clock divider can be synchronized using the external SYSREF± input signal. A valid SYSREF± resets the clock divider to a programmable state. This synchronization feature aligns the clock dividers of multiple devices, ensuring simultaneous input sampling.

9.11 Clock Jitter Considerations

High-speed, high-resolution ADCs are very sensitive to the quality of the clock input signal. At a given input frequency (fA), the SNR degradation due solely to aperture jitter (tJ) is given by:

$$SNR = -20 \times log10\ (2 \times \pi \times fA \times tJ)$$

where the rms aperture jitter represents the rms sum of all jitter sources, including the clock input signal, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter.

(See Chinese Datasheet Page 17)

Figure 18: Ideal SNR vs. Input Frequency and Jitter

When aperture jitter can affect the dynamic range of the JXA011, the clock input signal should be treated as an analog signal. The clock driver supply should be separated from the ADC output driver supply to avoid coupling digital noise into the clock signal. If the clock signal comes from another type of clock source (via gating, division, or other methods), the original clock must be used for retiming in the final stage.

9.12 Power-Down / Standby Mode

The JXA011 has a PDWN/STBY pin that can be used to configure the device for power-down or standby mode. The default configuration is PDWN. The PDWN/STBY pin is a logic-high input. In power-down mode, the JESD204B link is interrupted. Power-down options can also be set via Register 0x03F and Register 0x040. In standby mode, the JESD204B link is not interrupted, and zeros are transmitted for all converter samples. This can be changed by selecting the /K/ character using bit 7 of Register 0x571.

9.13 Temperature Diode

The JXA011 includes a diode-based temperature sensor for measuring chip temperature. This diode outputs a voltage that acts as a regular temperature sensor to monitor internal chip temperature. Via SPI, the temperature diode voltage can be output to the FD_A pin. The diode can be enabled or disabled through bit 0 of Register 0x028. Register 0x028 is a local register. To enable temperature diode readout, Channel A must be selected in the device index register (0x008). By setting Register 0x040[2:0], the FD_A pin is configured to output the diode voltage.

(See Chinese Datasheet Page 17)

Figure 19: Temperature Diode Voltage vs. Temperature

9.14 ADC Overrange and Fast Detect

In receiver applications, a reliable mechanism is required to determine when the converter is clipping. The standard overrange bit in the JESD204B output provides limited information about the analog input status.

Therefore, it is desirable to set a programmable threshold below full scale to reduce gain before clipping occurs. Additionally, because the slew rate of the input signal can be very high, the latency of this function is critical. However, high-speed, high-accuracy pipelined converters have significant latency. The JXA011 has built-in detection circuitry that each channel can use to monitor thresholds and assert the FD_A and FD_B pins.

9.14.1 ADC Overrange

When an overrange is detected at the ADC input, the ADC overrange indicator is set. The overrange indicator can be embedded as a control bit in the JESD204B link (when CSB > 0). The delay of this overrange indicator matches the sample delay. The JXA011 can also record overrange conditions for any of the 8 virtual converters. The overrange status of each virtual converter is recorded as a flag bit in Register 0x563. The contents of Register 0x563 can be cleared using Register 0x562 by toggling the bit corresponding to the virtual converter between set and reset positions.

(See Chinese Datasheet Page 17)

Figure 20: FD_A and FD_B Threshold Settings

9.14.2 Fast Threshold Detect (FD_A and FD_B)

The FD bit is immediately set to 1 whenever the absolute value of the input signal exceeds the programmable upper threshold. The FD bit is only cleared to 0 when the absolute value of the input signal drops below the lower threshold and remains below for longer than the programmable dwell time. This feature provides hysteresis to prevent the FD bit from toggling too frequently.

The upper and lower threshold registers and the dwell time register operation are shown in Figure 20. When the input signal amplitude exceeds the setting of the fast-detect upper threshold register (Registers 0x247 and 0x248), the FD indicator is set. The value of the selected threshold register is compared with the signal amplitude at the ADC output. Fast upper-threshold detection has a maximum latency of 28 clock cycles. The approximate upper-threshold amplitude is defined by:

$$\textit{Upper Threshold Amplitude (dBFS)} = 20 \times \log(\textit{threshold amplitude} / 2^{13})$$

The FD indicator does not clear until the signal drops below the lower threshold and remains below for longer than the set dwell time. The lower threshold is set in the fast-detect lower threshold register (Registers 0x249 and 0x24A).

For example, to set an upper threshold of –6 dBFS, write 0xFFF to Registers 0x247 and 0x248. To set a lower threshold of –10 dBFS, write 0xA1D to Registers 0x249 and 0x24A. The dwell time can be set from 1 to 65,535 sampling clock cycles by writing the desired value to the fast-detect dwell time register (Registers 0x24B and 0x24C).

9.15 Digital Down-Converter (DDC)

The JXA011 has four built-in digital down-converters (DDC 0 through DDC 3) for filtering and reducing the output data rate. The digital processing section includes an NCO, half-band decimation filters, FIR filters, gain stages, and complex-to-real conversion stages. Each processing module has control lines that can be individually enabled or disabled to provide the required processing function. By configuring the DDC, real or complex data can be output.

9.15.1 DDC I/Q Input Selection

The JXA011 has 2 ADC channels and 4 DDC channels. Each DDC channel has 2 input ports that can be paired to support real or complex input through an I/Q crossbar multiplexer. For real signals, both DDC input ports must select the same ADC channel (e.g., DDC input port I = ADC Channel A, input port Q = ADC Channel A). For complex signals, each DDC input port must select a different ADC channel (e.g., DDC input port I = ADC Channel A, input port Q = ADC Channel B). The input of each DDC is controlled by the DDC input selection register (Register 0x311, 0x331, 0x351, and 0x371).

9.15.2 DDC I/Q Output Selection

Each DDC channel has 2 output ports that can be paired to support real or complex output. For real output signals, only DDC output port I is used (DDC output port Q is inactive). For complex I/Q output signals, both DDC output port I and DDC output port Q are used. The I/Q output of each DDC channel is controlled by the DDC complex-to-real enable bit (bit 3) in the DDC control register (Register 0x310, 0x330, 0x350, and 0x370).

The chip Q ignore bit (bit 5) in the chip application mode register (Register 0x200) controls the chip output multiplexing for all DDC channels. When all DDC channels use real output, this bit must be set high to ignore all DDC Q output ports. When any DDC channel is configured to use complex I/Q output, this bit must be cleared to use both DDC output ports I and Q.

9.15.3 DDC Overview

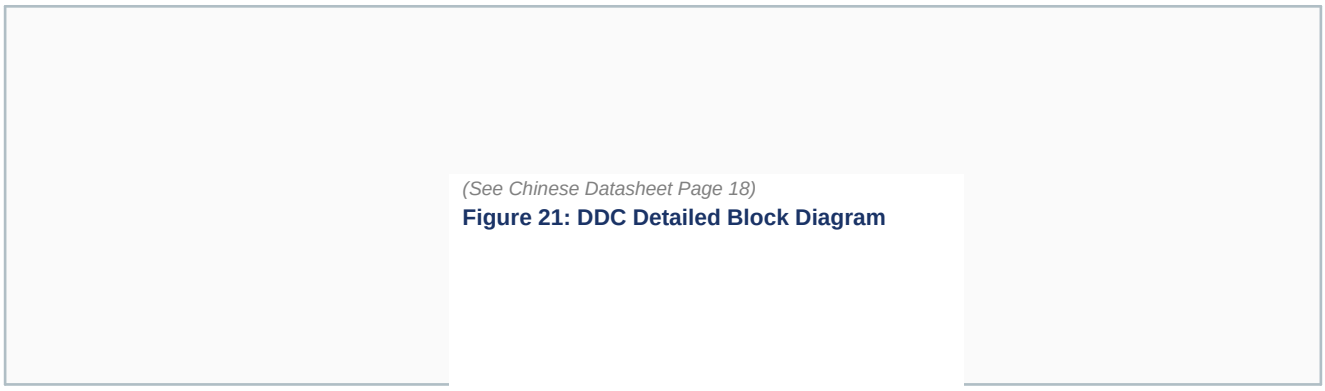
The four DDC modules are used to extract a portion of the full digital spectrum captured by the ADC. They are designed for IF sampling or oversampled baseband radios requiring wideband input signals. Each DDC module contains four signal processing stages:

Frequency Conversion Stage (optional): Consists of a 12-bit complex NCO and quadrature mixer, used for frequency conversion of real or complex input signals. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage: After down-conversion to baseband, the filtering stage decimates the spectrum using up to four cascaded half-band low-pass filters for rate conversion. The decimation process reduces the output data rate, which in turn reduces the output interface rate.

Gain Stage (optional): Real input signals down-mixed to baseband experience a 6 dB loss; the gain stage compensates by adding 0 dB or 6 dB of gain.

Complex-to-Real Conversion Stage (optional): When real output is required, the complex-to-real conversion stage performs an fS/4 mixing operation and filters out the complex component of the signal, converting the complex output back to real output.



(See Chinese Datasheet Page 18)

Figure 21: DDC Detailed Block Diagram

(See Chinese Datasheet Page 19)

Figure 22: DDC Operating Principle

9.16 Frequency Translation

9.16.1 Overview

Frequency translation is implemented using a 12-bit complex NCO and digital quadrature mixer. Frequency translation converts a real or complex input signal from intermediate frequency (IF) to baseband complex digital output (carrier = 0 Hz). The frequency translation stage of each DDC can be individually controlled, supporting four different IF modes. The mode is selected using bits [5:4] of the DDC control register (Register 0x310, 0x330, 0x350, and 0x370):

- Variable IF mode
- 0 Hz IF (ZIF) mode
- fS/4 Hz IF mode
- Test mode

(See Chinese Datasheet Page 19)

Figure 23: NCO FTW Selection — Real Input

(See Chinese Datasheet Page 20)

Figure 24: NCO FTW Selection — Complex Input

9.16.2 DDC NCO Plus Mixer Loss and SFDR

When a real input signal is down-mixed to baseband, there is a 6 dB loss due to filtering of the negative image. Additionally, the NCO introduces 0.05 dB of loss. The total loss for a real input signal down-mixed to baseband is 6.05 dB. Therefore, users are advised to enable the additional 6 dB gain in the DDC gain stage to compensate for this loss, re-centering the dynamic range of the signal in the full-scale output bits.

When a complex input signal is down-mixed to baseband, the maximum value each I/Q sample can achieve after passing through the complex mixer is 1.414 × full-scale. For complex signals, to prevent I/Q samples from overranging and to keep the data bit width consistent with real mixing, the mixer introduces 3.06 dB of loss (0.707 × full-scale). Additionally, the NCO introduces 0.05 dB of loss. The total loss for a complex input signal down-mixed to baseband is –3.11 dB.

For all output frequencies, the worst-case SFDR of the NCO output spurious signals is greater than 102 dBc.

9.16.3 Numerically Controlled Oscillator (NCO)

Each DDC of the JXA011 has a 12-bit NCO to support the frequency translation process. The NCO can shift the input spectrum to dc, which is then effectively filtered by subsequent filters to prevent signal aliasing. The NCO can be set via the frequency tuning word (FTW) and phase offset word (POW).

9.16.4 Setting the NCO FTW and POW

The NCO frequency value is determined by the 12-bit two's-complement number input to the NCO FTW. The following frequency words represent frequency values between –fS/2 and +fS/2 (excluding +fS/2):

- 0x800 represents a frequency of –fS/2
- 0x000 represents dc (0 Hz frequency)
- 0x7FF represents a frequency of +fS/2 – fS/2^{12}

The NCO frequency tuning word can be calculated using:

$$NCO\_FTW = round(2^{12} \times Mod(fC, fS) / fS)$$

where NCO_FTW is the 12-bit two's-complement value representing the NCO FTW; fS is the JXA011 sampling frequency (clock rate) in Hz; fC is the desired carrier frequency in Hz; Mod( ) is the modulo function; and round( ) is

the rounding function.

9.16.5 NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW) that determines the instantaneous phase of the NCO. The initial reset value of each PAW is determined by the POW. The phase increment value of each PAW is determined by the FTW.

There are two methods for synchronizing multiple PAWs within a chip: (1) using SPI — the DDC NCO soft-reset bit in the DDC sync control register (bit 4 of Register 0x300) can reset all PAWs in the chip; this method can only synchronize DDC channels within the same JXA011 chip. (2) Using the SYSREF± pin — if the SYSREF± pin is enabled through SYSREF± control registers (Register 0x120 and Register 0x121) and DDC sync is enabled through bits [1:0] of the DDC sync control register (Register 0x300), any subsequent SYSREF± event resets all PAWs in the chip; this method can synchronize DDC channels both within the same JXA011 chip and across multiple JXA011 chips.

9.16.6 Mixer

The NCO is accompanied by a mixer whose operation is similar to an analog quadrature mixer. It uses the NCO frequency as the local oscillator to down-convert the input signal (real or complex). For real input signals, this mixer performs a real mixer operation (using two multipliers). For complex input signals, this mixer performs a complex mixer operation (using four multipliers and two adders). The mixer adjusts its operation based on the input signal (real or complex) provided to each channel.

9.17 DDC Configuration Examples

Table 6 lists the register settings for several DDC configuration examples.

Table 6: DDC Configuration Examples

Chip App Mode	Chip Decimation	DDC Input	DDC Output	Bandwidth per DDC	Virtual Converters (M)	Register Settings
1 DDC	2	Complex	Complex	77% × fS	2	Reg 0x200 = 0x01; Reg 0x201 = 0x01; Reg 0x310 = 0x83; Reg 0x311 = 0x04; FTW & POW per DDC0
2 DDCs	4	Complex	Complex	38.5% × fS	4	Reg 0x200 = 0x02; Reg 0x201 = 0x02; Reg 0x310/330 = 0x80; Reg 0x311/331 = 0x04; FTW & POW per DDC
2 DDCs	4	Complex	Real	19.25% × fS	2	Reg 0x200 = 0x22; Reg 0x201 = 0x02; Reg 0x310/330 = 0x89; Reg 0x311/331 = 0x04; FTW & POW per DDC
2 DDCs	4	Real	Real	19.25% × fS	2	Reg 0x200 = 0x22; Reg 0x201 = 0x02; Reg 0x310/330 = 0x49; Reg 0x311 = 0x00, 0x331 = 0x05; FTW & POW per DDC
2 DDCs	4	Real	Complex	38.5% × fS	4	Reg 0x201 = 0x02; Reg 0x310/330 = 0x40; Reg 0x311 = 0x00, 0x331 = 0x05; FTW & POW per DDC
4 DDCs	8	Real	Complex	19.25% × fS	8	Reg 0x200 = 0x03; Reg 0x201 = 0x03; Reg 0x310/330/350/370 = 0x41; Reg 0x311/331 = 0x00, 0x351/371 = 0x05; FTW & POW per DDC
4 DDCs	16	Real	Complex	9.625% × fS	8	Reg 0x200 = 0x03; Reg 0x201 = 0x04; Reg 0x310/330/350/370 = 0x42; Reg 0x311/331 = 0x00, 0x351/371 = 0x05; FTW & POW per DDC

Notes: 1. fS = ADC sample rate. Listed bandwidth is for passband ripple < –0.001 dB and >100 dB stopband alias rejection. 2. After all writes to FTW or POW registers are complete, the NCO must be synchronized via SPI or SYSREF± pins. This is required for proper NCO operation.

10. Digital Output — JESD204B Interface

10.1 JESD204B Interface Overview

The JXA011 digital output is designed according to the JEDEC standard JESD204B ("SerDes Framer Interface for Data Converters"). JESD204B is the protocol by which the JXA011 connects to digital processing devices through a serial interface with lane rates up to 10 Gbps. Advantages of the JESD204B interface over LVDS include less board space for data interface routing and smaller packages for both the converter and logic device.

The JESD204B data transmitter module combines parallel data from the ADC into data frames and outputs serial data using 8B/10B encoding and optional data scrambling. During initial link establishment, special control characters are used to support lane synchronization; subsequent synchronization is maintained by additional control characters embedded in the data stream. Completing the serial link requires a JESD204B receiver.

The JXA011 JESD204B data transmitter module can map up to 2 physical ADCs or 8 virtual converters (when DDC is enabled) through the link. The link can be configured to use 1, 2, or 4 JESD204B lanes. The JESD204B specification references multiple parameters that define the link; these parameters must match between the JESD204B transmitter and receiver.

- L = number of lanes per link (JXA011 values: 1, 2, or 4)
- M = number of converters per link (JXA011 values: 1, 2, 4, or 8)
- F = number of octets per frame (JXA011 values: 1, 2, 4, 8, or 16)
- N' = number of bits per sample (JESD204B word size) (JXA011 values: 8 or 16)
- N = converter resolution (JXA011 values: 7 to 16)
- CS = number of control bits per sample (JXA011 values: 0, 1, 2, or 3)
- K = number of frames per multiframe (JXA011 values: 4, 8, 12, 16, 20, 24, 28, or 32)
- S = samples transmitted per converter per frame period (automatically set based on L, M, F, and N')
- HD = high-density mode (automatically set based on L, M, F, and N')
- CF = control words per frame clock cycle per converter (value is 0)

Figure 25 shows a simplified block diagram of the JXA011 JESD204B link. The default configuration uses two converters and four data lanes. Data from Converter A is output on SERDOUT0± and/or SERDOUT1±, and data from Converter B is output on SERDOUT2± and/or SERDOUT3±. The JXA011 supports other configurations, such as combining the outputs of both converters into a single lane or changing the mapping of the A and B digital output paths.

(See Chinese Datasheet Page 22)

Figure 25: Full-Bandwidth Mode Transmit Link Simplified Diagram

(See Chinese Datasheet Page 23)

Figure 26: ADC Output Data Path

10.2 Functional Overview

The block diagram in Figure 27 shows the JESD204B hardware data flow from sample input to physical output. Following the OSI model widely used to describe the abstract layers of communication systems, the processing can be divided into layers: transport layer, data link layer, and physical layer (serializer and output driver).

(See Chinese Datasheet Page 28)

Figure 27: Data Flow Diagram

10.2.1 Transport Layer

The transport layer is responsible for packaging data (including samples and optional control bits) into JESD204B frames for mapping into 8-bit words. These 8-bit words are sent to the data link layer. Tail bits are added as needed to fill gaps. The number of tail bits in a sample (JESD204B word) can be determined using: T = N' – N – CS

10.2.2 Data Link Layer

The data link layer is responsible for low-level functions of data transmission over the link, including scrambling data (optional), inserting control characters to support multi-chip synchronization/lane alignment/monitoring, and encoding 8-bit words into 10-bit symbols. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains link configuration data used by the receiver to verify transport layer settings.

10.2.3 Physical Layer

The physical layer consists of high-speed circuits with a clock frequency equal to the serial clock rate. In this layer, parallel data is converted into 1, 2, or 4 lanes of high-speed differential serial data.

10.3 JESD204B Link Establishment

The JXA011 JESD204B transmitter (Tx) interface operates in Subclass 1 as specified in JEDEC Standard 204B. The link establishment process consists of several steps: code group synchronization and SYNCINB±, initial lane alignment sequence (ILAS), and user data and error correction.

10.3.1 Code Group Synchronization (CGS) and SYNCINB±

CGS is the process by which the JESD204B receiver finds the boundaries between 10-bit symbols in the data stream. During the CGS phase, the JESD204B transmit module transmits /K28.5/ characters. The receiver must use clock and data recovery (CDR) techniques to locate /K28.5/ characters in the input data stream.

The receiver asserts the SYNCINB± pin of the JXA011 low to issue a synchronization request. The JESD204B Tx then starts sending /K/ characters. Once the receiver has synchronized—after correctly receiving at least four consecutive /K/ symbols—it deasserts SYNCINB±. The JXA011 then sends an ILAS at the next local multiframe clock (LMFC) boundary.

10.3.2 Initial Lane Alignment Sequence (ILAS)

The CGS phase is followed by the ILAS phase, which begins at the next LMFC boundary. The ILAS consists of four multiframes, starting with an /R/ character and ending with an /A/ character.

(See Chinese Datasheet Page 29)

Figure 28: Initial Lane Alignment Sequence

10.3.3 User Data and Error Detection

After completing the initial lane alignment sequence, user data is transmitted. In general, all data within a frame is considered user data. However, to monitor frame clock and multiframe clock synchronization, there is a mechanism to replace characters with /F/ or /A/ alignment characters when data meets certain conditions. These conditions differ for unscrambled and scrambled data. Scrambling is enabled by default but can be disabled via SPI.

10.4 Digital Output, Timing, and Control

The JXA011 physical layer consists of drivers specified by JEDEC Standard 204B (July 2011). Differential digital outputs are powered on by default. Each driver uses a 100 Ω dynamic internal termination resistor to reduce reflected interference. Placing a 100 Ω differential termination resistor at the input of each receiver achieves a nominal receiver swing of 300 mV p-p. A single-ended 50 Ω termination resistor can also be used.

(See Chinese Datasheet Page 35)

Figure 29: AC-Coupled Digital Output Termination

(See Chinese Datasheet Page 36)

Figure 30: DC-Coupled Digital Output Termination

The JXA011 digital output can interface with custom ASIC and FPGA receivers, providing excellent switching performance in high-noise environments. A single point-to-point network topology is recommended, with a single 100 Ω differential termination resistor placed as close to the receiver input as possible.

10.5 Deemphasis

When interconnect insertion loss does not meet the JESD204B specification, deemphasis can be used to meet the receiver eye mask. Deemphasis should only be used when the receiver cannot recover the clock due to excessive insertion loss. In general, this feature is disabled to save power. Additionally, enabling and setting too high a deemphasis value for a short link can cause the receiver eye to fail. Deemphasis settings should be used cautiously as they increase EMI.

10.6 Phase-Locked Loop (PLL)

A phase-locked loop (PLL) is used to generate the serializer clock, which operates at the JESD204B lane rate. The PLL lock status can be checked via the PLL lock status bit (bit 7 of Register 0x56F). This read-only bit tells the user whether PLL lock has been achieved for a particular setting. The JESD204B lane rate control (bit 4 of Register 0x56E) must be set to correspond to the lane rate.

10.7 JESD204B Tx Converter Mapping

To support different chip operating modes, the JXA011 design treats each sample stream (real or I/Q) as coming from a different virtual converter. I/Q samples are always mapped in pairs, with the I sample mapped to the first virtual converter and the Q sample mapped to the second. With this transport layer mapping, the number of virtual converters is the same in various cases.

(See Chinese Datasheet Page 36)

Figure 31: I/Q Transport Layer Mapping

(See Chinese Datasheet Page 37)

Figure 32: DDC and Virtual Converter Mapping

10.8 Configuring the JESD204B Link

The JXA011 has one JESD204B link. It is easily configured via the JESD204B quick configuration register (Register 0x570). The serial outputs (SERDOUT0± through SERDOUT3±) are part of one JESD204B link. The basic parameters that determine the link setup include: the number of lanes per link (L), the number of converters per link (M), and the number of octets per frame (F).

The lane line rate is related to the JESD204B parameters as follows:

$$Lane\ Line\ Rate = (M \times N' \times (10/8) \times fOUT) / L$$

where fOUT = fADC_clock / Decimation Ratio.

The output can be configured using the following steps:

1. Power down the link.
2. Select the quick configuration option.
3. Configure detailed options.
4. Set output lane mapping (optional).
5. Set other driver configuration options (optional).
6. Power up the link.

10.9 Timing Specifications

Table 7: Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
tSU_SR	Device clock to SYSREF+ setup time	117	—	—	ps
tH_SR	Device clock to SYSREF+ hold time	—	—	–96	ps
tDS	Data setup time before SCLK rising edge	3	—	—	ns
tDH	Data hold time after SCLK rising edge	3	—	—	ns
tCLK	SCLK period	40	—	—	ns
tS	Setup time between CSB and SCLK	3	—	—	ns
tH	Hold time between CSB and SCLK	3	—	—	ns
tHIGH	Minimum SCLK high time	10	—	—	ns
tLOW	Minimum SCLK low time	10	—	—	ns
tEN_SDIO	SDIO pin switch time from input to output (relative to SCLK falling edge)	—	—	10	ns
tDIS_SDIO	SDIO pin switch time from output to input (relative to SCLK rising edge)	—	—	10	ns

(See Chinese Datasheet Page 39)

Figure 33: Data Output Timing (Full-Bandwidth Mode, L=4, M=2, F=1)

(See Chinese Datasheet Page 39)

Figure 34: SYSREF± Setup/Hold Timing

(See Chinese Datasheet Page 40)

Figure 35: SPI Timing

11. Product Marking

(See Chinese Datasheet Page 41)

Figure 36: Product Marking Diagram

12. Assembly and Handling Instructions

12.1 PCB Layout Considerations

- The application board must have a complete, clean ground plane.
- The application board should be a multilayer board with a dedicated ground plane.
- Digital ground and analog ground on the application board should be separated as much as possible. Do not route digital traces next to analog traces or beneath the ADC.
- High-quality ceramic bypass capacitors must be connected to the supplies, placed as close to the pins as possible. Traces connecting pins to bypass capacitors should be as short and wide as possible.

12.2 Application Notes

- Differential inputs should be routed close together and parallel to each other.
- Input traces should be as short as possible to minimize parasitic capacitance and noise coupling.
- Pay attention to ambient temperature and ensure adequate thermal dissipation during operation. For optimal thermal and electrical performance, the device's exposed pad must be soldered to a large ground plane on the PCB.
- The device ground should be connected to the PCB ground plane through as many vias and with as much area as possible.
- Refer to the timing diagrams for the relationship between output data, output clock, and analog input.
- No specific power-up sequence is required; power-up settling time is less than 10 ms. Unused input/output pins may be left floating. The thermal pad must be grounded. No potential is required for the lid.
- It is recommended to reset the device after power-up (write 0x81 to Register 0x000) before normal operation.

12.3 ESD Precautions

Electrostatic charges can easily accumulate on the human body and test equipment, and may discharge without detection. Although this product has dedicated ESD protection circuitry, permanent device damage can occur during high-energy electrostatic discharge. Therefore, appropriate ESD precautions are recommended to avoid device performance degradation or loss of function. ESD sensitivity class: Class 1B (HBM 500 V).

Operation beyond absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; operation at these or any other conditions beyond those indicated in the operational sections is not implied. Extended exposure to absolute maximum rating conditions may affect device reliability.

12.4 Thermal Recommendations

- It is recommended that the user enhance heat dissipation during operation, e.g., by covering the top of the device with thermal grease and a metal heat sink (which can be shared with surrounding components). A fan

can be added if available, as shown in Figure 37.

• For PCB layout, it is recommended to divide the package thermal pad into 4 or 9 grid sections to improve soldering coverage, as shown in Figure 38.

(See Chinese Datasheet Page 44)

Figure 37: Recommended Heat Sink Design

(See Chinese Datasheet Page 45)

Figure 38: Recommended PCB Thermal Pad Design

12.5 Storage and Soldering Requirements

• **Moisture Sensitivity:** This product has a moisture sensitivity level of MSL3. After removing the product from the moisture barrier bag, the allowable exposure time before reflow is ≤168 hours at ≤30°C / 60% RH (floor life).

• **Baking:** Before assembly, it is recommended to bake at 125°C for 24 hours to remove internal moisture. (Note: After baking, the environment is particularly dry and prone to static electricity; ESD protection is required.)

• **SnPb Reflow:** Board-level assembly recommends SnPb reflow (Sn63Pb37). Recommended peak temperature range: 210°C to 220°C. Maximum peak temperature: ≤245°C. Time above liquidus: 60 to 90 s. Ramp-up rate: ≤3°C/s. Ramp-down rate: ≤6°C/s.

• **Pb-Free Reflow:** If using Pb-free reflow (SAC305), recommended peak temperature range: 230°C to 245°C. Maximum peak temperature: ≤260°C. Time above liquidus: 60 to 90 s. Ramp-up rate: ≤3°C/s. Ramp-down rate: ≤6°C/s.

• **Mixed Assembly:** If mixed board-level assembly processes require higher temperatures, ensure the device body temperature does not exceed 260°C. (Measurement point is the top surface of the device during reflow.)

• **Pad Finish:** The pad plating is electroless nickel palladium gold (ENEPIG), with a gold layer thickness of 0.075 μm. Solder dipping is not required. If forced solder dipping is required, follow the standard QJ3267-2006; ensure the device body temperature does not exceed 260°C.

• **Side Pads:** Side pads of this product are bare copper; no additional soldering is required, per IPC-A-610H 8.3.13.

13. Troubleshooting Guide

Symptom	Possible Cause / Action
No signal output	Check power supply voltages, input signal, and clock for correct application.
Overflow / clipping signal	Check that the voltage reference is operating normally and that the input signal amplitude is correct.
Unstable device operation	Check the power supply; ensure the supply voltage is stable.

14. Comparison with Reference Device (AD9680-1000)

Table 8 provides a comparison of key electrical parameters between the JXA011 and the Analog Devices AD9680-1000 reference device.

Table 8: JXA011 vs. AD9680-1000 Parameter Comparison

Parameter	Symbol	Unit	JXA011	AD9680-1000
Temperature range	TC	°C	–40 to 85	25
Resolution	RES	bits	14	14
Number of channels	NCH	CH	2	2
Power consumption	PW	W	Max ≤4.0, Typ 3.3	Typ 3.3
Differential nonlinearity	DNL	LSB	Max ±2.0, Typ ±0.8	–0.7 to +0.8
Integral nonlinearity	INL	LSB	Max ±12, Typ ±3.5	–5.7 to +6.9
Reference output voltage	VREF	mV	950–1050, Typ 1000	Typ 1000
Sample rate	FS	MSPS	1000	1000
SNR (fIN = 10 MHz)	SNR	dBFS	≥60.0, Typ 66.6 @25°C	Typ 67.2 @25°C
SNR (fIN = 170 MHz)	SNR	dBFS	≥59.5, Typ 66.4 @25°C	Typ 66.6 @25°C
SNR (fIN = 450 MHz)	SNR	dBFS	≥59.2, Typ 63.7 @25°C	Typ 64.0 @25°C
SNR (fIN = 765 MHz)	SNR	dBFS	≥59.1, Typ 62.8 @25°C	Typ 62.6 @25°C
SINAD (fIN = 10 MHz)	SINAD	dBFS	≥59.5, Typ 66.4 @25°C	Typ 67.1 @25°C
SINAD (fIN = 170 MHz)	SINAD	dBFS	≥59, Typ 66.2 @25°C	Typ 66.4 @25°C
SINAD (fIN = 450 MHz)	SINAD	dBFS	≥58, Typ 62.7 @25°C	Typ 63.8 @25°C
SINAD (fIN = 765 MHz)	SINAD	dBFS	≥57.5, Typ 61.8 @25°C	Typ 62.5 @25°C
ENOB (fIN = 10 MHz)	ENOB	Bits	≥9.59, Typ 10.7 @25°C	Typ 10.8 @25°C
ENOB (fIN = 170 MHz)	ENOB	Bits	≥9.50, Typ 10.7 @25°C	Typ 10.7 @25°C
ENOB (fIN = 450 MHz)	ENOB	Bits	≥9.34, Typ 10.1 @25°C	Typ 10.3 @25°C
ENOB (fIN = 765 MHz)	ENOB	Bits	≥9.25, Typ 9.9 @25°C	Typ 10.0 @25°C
SFDR (fIN = 10 MHz)	SFDR	dBFS	≥70, Typ 88 @25°C	Typ 88 @25°C
SFDR (fIN = 170 MHz)	SFDR	dBFS	≥69, Typ 82 @25°C	Typ 85 @25°C
SFDR (fIN = 450 MHz)	SFDR	dBFS	≥66, Typ 79 @25°C	Typ 82 @25°C
SFDR (fIN = 765 MHz)	SFDR	dBFS	≥66, Typ 77 @25°C	Typ 82 @25°C
HD2,3 (fIN = 10 MHz)	HD2,3	dBFS	≤–70, Typ –88 @25°C	Typ –88 @25°C
HD2,3 (fIN = 170 MHz)	HD2,3	dBFS	≤–69, Typ –82 @25°C	Typ –85 @25°C
HD2,3 (fIN = 450 MHz)	HD2,3	dBFS	≤–66, Typ –79 @25°C	Typ –82 @25°C
HD2,3 (fIN = 765 MHz)	HD2,3	dBFS	≤–66, Typ –77 @25°C	Typ –82 @25°C
Logic input high voltage	VIH	V	≥0.8 × VSPIVDD	≥0.8 × VSPIVDD
Logic input low voltage	VIL	V	0 to 0.5	0 to 0.5
Logic output high voltage (SDIO)	VOH	V	≥0.8 × VSPIVDD	≥0.8 × VSPIVDD
Logic output low voltage (SDIO)	VOL	V	0 to 0.5	0 to 0.5

Parameter	Symbol	Unit	JXA011	AD9680-1000
JESD204B interface rate	fSERDES	Gbps	≤10	≤10

Note: Input range and input buffer configured per recommended settings for the corresponding frequency band.

15. Additional Information

15.1 Document Revision History

Revision	Date	Changed Sections	Description
1.0	2024-05-29	—	Initial release
1.1 (V.20250708)	2025-07-08	—	Added recommendation to reset device after power-up (write 0x81 to Register 0x000) before normal operation

15.2 Product Status

■ Production (this product model is currently in production and can be supplied as a formal product).